IN THE CLAIMS

1. (Original) A multi-function driver configurable to process either single-ended or differential signals, comprising:

a first pull-up circuit coupled between a supply voltage and a first output terminal, and including a first terminal to receive a first input signal, a second terminal to receive a first bias voltage, and a third terminal;

a second pull-up circuit coupled between the supply voltage and a second output terminal, and including a first terminal to receive a second input signal, a second terminal to receive the first bias voltage, and a third terminal;

a first pull-down circuit coupled between the first output terminal and ground potential, and including a first terminal to receive the first input signal, a second terminal to receive a second bias voltage, and a third terminal;

a second pull-down circuit coupled between the second output terminal and ground potential, and including a first terminal to receive the second input signal, a second terminal to receive the second bias voltage, and a third terminal;

a first switch connected between the third terminals of the first and second pull-up circuits, the first switch responsive to a mode signal; and

a second switch connected between the third terminals of the first and second pull-down circuits, the second switch responsive to the mode signal.

2. (Original) The driver of Claim 1, wherein the mode signal determines whether the driver is configured to process single-ended signals or configured to process differential signals.

3. (Original) The driver of Claim 1, wherein:

the first pull-up circuit and the first pull-down circuit are configured to implement a first inverter and the second pull-up circuit and the second pull-down circuit are configured to implement a second inverter when the mode signal is in a first logic state; and

the first and second pull-up circuits are configured to implement a first differential circuit and the first and second pull-down circuits are configured to implement a second differential circuit when the mode signal is in a second logic state.

4. (Original) The driver of Claim 3, wherein:

setting the mode signal to the first logic state configures the driver as a high-speed transceiver logic (HSTL) driver; and

setting the mode signal to the second logic state configures the driver as a low-voltage differential signaling (LVDS) driver.

5. (Original) The driver of Claim 1, further comprising:

a common mode voltage circuit selectively connected between the first and second output terminals in response to the mode signal.

6. (Original) The driver of Claim 5, wherein the common mode voltage circuit is not coupled between the first and second output terminals when the mode signal is in a first logic state, and the common mode voltage circuit is coupled between the first and second output terminals when the mode signal is in a second logic state.

7. (Original) The driver of Claim 5, wherein the common mode circuit comprises:

a first resistor and a third switch connected in series between the first output terminal and a common mode voltage node, the third switch responsive to the mode signal; and

a second resistor and a fourth switch connected in series between the second output terminal and the common mode voltage node, the second switch responsive to the mode signal.

8. (Original) The driver of Claim 1, wherein the first and second pull-up circuits each comprise:

a first PMOS transistor connected in series between the supply voltage and the third terminal of the corresponding pull-up circuit, and having a gate responsive to the first bias voltage; and

a second PMOS transistor connected in series between the third terminal and the output terminal of the corresponding pull-up circuit, and having a gate responsive to the corresponding input signal.

9. (Original) The driver of Claim 8, wherein the first and second pull-up circuits each further comprise:

a third PMOS transistor connected in parallel with the first PMOS transistor and having a gate to receive either the first bias voltage or a modified bias voltage in response to the mode signal.

10. (Original) The driver of Claim 9, further including a bias circuit, comprising:

a fourth PMOS transistor connected in series between the supply voltage and the gate of the first PMOS transistor, and having a gate responsive to the mode signal;

a first NMOS transistor connected in series between the gates of the first and third PMOS transistors, and having a gate responsive to the mode signal;

a second NMOS transistor connected in series between the gate of the third PMOS transistor and ground potential, and having a gate responsive to the mode signal;

a first resistor connected between the supply voltage and the gate of the first PMOS transistor; and

a second resistor connected between the gate of the first PMOS transistor and ground potential.

11. (Original) The driver of Claim 1, wherein the first and second pull-down circuits each comprise:

a first NMOS transistor connected in series between the third terminal of the corresponding pull-down circuit and ground potential, and having a gate responsive to the second bias voltage; and

a second NMOS transistor connected in series between the output terminal and the third terminal of the corresponding pull-down circuit, and having a gate responsive to the corresponding input signal.

12. (Original) The driver of Claim 11, wherein the first and second pull-down circuits each further comprise:

a third NMOS transistor connected in parallel with the first NMOS transistor and having a gate to receive either the second bias voltage or a modified bias voltage in response to the mode

signal.

13. (Original) The driver of Claim 12, wherein the driver further includes a bias circuit, comprising:

a fourth NMOS transistor connected in series between the gate of the first NMOS transistor and ground potential, and having a gate responsive to the mode signal;

a first PMOS transistor connected in series between the gates of the first and third NMOS transistors, and having a gate responsive to the mode signal;

a second PMOS transistor connected in series between the gate of the third PMOS transistor and the supply voltage, and having a gate responsive to the mode signal;

a first resistor connected between the supply voltage and the gate of the first NMOS transistor; and

a second resistor connected between the gate of the first NMOS transistor and ground potential.

14. (Cancelled)

15. (Currently Amended) ~~The driver of Claim 14,~~ A multi-function driver configurable to process either single-ended or differential signals, comprising:

first and second circuits connected in series between a supply voltage and ground potential, the first and second circuits each having an input to receive a first input signal and having a first common output to provide a first output signal;

third and fourth circuits connected in series between the supply voltage and ground potential, the third and fourth circuits each having an input to receive a second input signal and having a second common output to provide a second output signal;

a first switch to selectively connect the first and third circuits together in response to a mode signal; and

a second switch to selectively connect the second and fourth circuits together in response to the mode signal, wherein the mode signal indicates whether the driver is configured to process single-ended signals or differential signals.

16. (Currently Amended) The driver of Claim ~~14~~ 15, wherein:

the first and second circuits implement a first inverter and the third and fourth circuits implement a second inverter to simultaneously process two single-ended signals when the mode signal is in a first logic state; and

the first and third circuits implement a first differential circuit and the second and fourth circuits implement a second differential circuit to process a differential signal when the mode signal is in a second logic state.

17. (Currently Amended) The driver of Claim ~~14~~ 15, further comprising:

a common mode voltage circuit selectively connected between the first and second common outputs in response to the mode signal.

18. (Original) The driver of Claim 17, wherein the common mode voltage circuit is not coupled between the first and second common outputs when the mode signal is in a first logic state, and the common mode voltage circuit is coupled between the first and second common outputs when the mode signal is in a second logic state.

19. (Currently Amended) The driver of Claim ~~14~~ 15, wherein the first circuit comprises:

a first PMOS transistor connected in series between the supply voltage and a first terminal of the first switch, and having a gate coupled to a first bias node;

a second PMOS transistor connected in series between the first terminal of the first switch and the first common output, and having a gate responsive to the first input signal; and

a third PMOS transistor connected in parallel with the first PMOS transistor, and having a gate coupled to a second bias node.

20. (Original) The driver of Claim 19, wherein the third circuit comprises:

a fourth PMOS transistor connected in series between the supply voltage and a second terminal of the first switch, and having a gate coupled to the first bias node;

a fifth PMOS transistor connected in series between the second terminal of the first switch and the second common output, and having a gate responsive to the second input signal;

and

a sixth PMOS transistor connected in parallel with the fourth PMOS transistor, and having a gate coupled to the second bias node.

21. (Original) The driver of Claim 20, further comprising:

a bias circuit having first outputs coupled to the first and second bias nodes, the bias circuit providing the same bias voltage to the first and second bias nodes when the mode signal is in a first logic state and providing different bias voltages to the first and second bias nodes when the mode signal is in a second logic state.

22. (Original) The driver of Claim 21, wherein the second circuit comprises:

a first NMOS transistor connected in series between a first terminal of the second switch and ground potential, and having a gate coupled to a third bias node;

a second NMOS transistor connected in series between the first common output and the first terminal of the second switch, and having a gate responsive to the first input signal; and

a third NMOS transistor connected in parallel with the first NMOS transistor, and having a gate coupled to a fourth bias node.

23. (Original) The driver of Claim 22, wherein the fourth circuit comprises:

a fourth NMOS transistor connected in series between a second terminal of the second switch and ground potential, and having a gate coupled to the third bias node; and

a fifth NMOS transistor connected in series between the second common output and the second terminal of the second switch, and having a gate responsive to the second input signal; and

a sixth NMOS transistor connected in parallel with the fourth NMOS transistor, and having a gate coupled to the fourth bias node.

24. (Original) The driver of Claim 23, wherein the bias circuit has second outputs coupled to the third and fourth bias nodes, the bias circuit providing the same bias voltage to the third and fourth bias nodes when the mode signal is in a first logic state and providing different bias voltages to the third and fourth bias nodes when the mode signal is in a second logic state.

25. (Original) A driver for processing single-ended and differential signals, comprising:

first and second circuits connected in series between a supply voltage and ground potential;

third and fourth circuits connected in series between the supply voltage and ground potential;

means for configuring the first and second circuits to implement a first inverter and configuring the third and fourth circuits to implement a second inverter to simultaneously process two single-ended signals during a first mode; and

means for configuring the first and third circuits to implement a first differential circuit and configuring the second and fourth circuits to implement a second differential circuit to process a differential signal during a second mode.

26. (Original) The driver of Claim 25, further comprising:

means for isolating the first and third circuits from each other and for isolating the second and fourth circuits from each other during the first mode; and

means for connecting the first and third circuits together and for connecting the second and fourth circuits together during the second mode.

27. (Original) The driver of Claim 25, further comprising:

means for biasing the first and third circuits with a first bias voltage and for biasing the second and fourth circuits with a second bias voltage during the first mode; and

means for biasing the first and third circuits with a third bias voltage and for biasing the second and fourth circuits with a fourth bias voltage during the second mode.

28. (Original) A method of processing single-ended and differential signals using a multi-function driver having first, second, third, and fourth circuits, comprising:

configuring the first and second circuits to implement a first inverter and configuring the third and fourth circuits to implement a second inverter to simultaneously process two single-ended signals when a mode signal is in a first logic state; and

configuring the first and third circuits to implement a first differential circuit and

configuring the second and fourth circuits to implement a second differential circuit to process a differential signal when the mode signal is in a second logic state.

29. (Original) The method of Claim 28, further comprising:

isolating the first and third circuits from each other and isolating the second and fourth circuits from each other when the mode signal is in the first logic state; and

connecting the first and third circuits together and connecting the second and fourth circuits together when the mode signal is in the second logic state.

30. (Original) The method of Claim 28, further comprising:

biasing the first and third circuits with a first bias voltage and biasing the second and fourth circuits with a second bias voltage when the mode signal is in the first logic state; and

biasing the first and third circuits with a third bias voltage and biasing the second and fourth circuits with a fourth bias voltage when the mode signal is in the second logic state.

31. (Original) A method of processing single-ended and differential signals, comprising:

providing first and second circuits connected in series between a supply voltage and ground potential;

providing third and fourth circuits connected in series between the supply voltage and ground potential;

providing a first input signal to the first and second circuits;

providing a second input signal to the third and fourth circuits;

configuring the first and second circuits to implement a first inverter and configuring the third and fourth circuits to implement a second inverter to simultaneously process the first and second input signals as independent single-ended signals when a mode signal is in a first logic state; and

configuring the first and third circuits to implement a first differential circuit and configuring the second and fourth circuits to implement a second differential circuit to process the first and second input signals as differential signal when the mode signal is in a second logic state.

Rejection of Claims under 35 USC §102

Claim14 is rejected under 35 USC §102(b) as being anticipated by Okada (USP 5,959,854). Claim 14 has been cancelled, and thus the rejection of Claim 14 is now moot.

Objection to Claims

Claims 15-24 are objected to as being dependent upon a rejected base claim, but would be allowable if re-written in independent form to include the limitations of the base claim and any intervening claims.

Claim 15 has been re-written in independent form to include the limitations of base claim 14, and therefore is now patentable over the cited references.

Claims 16-24 depend from Claim 15 and therefore distinguish over the cited references for at least the same reasons as Claim 15.

Allowable Subject Matter

Claims 1-13 and 25-31 are allowable over the cited references.

CONCLUSION

In light of the above remarks, it is believed that Claims 1-13 and 15-31 are in condition for allowance and, therefore, a Notice of Allowance of Claims 1-13 and 15-31 is respectfully requested. If the Examiner's next action is other than allowance as requested, the Examiner is requested to call the undersigned at (415) 291-9497.

Respectfully submitted,

Dated: June 22, 2004

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CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Arlington, VA 22313 on June 22, 2004.

By: _____
William L Paradice III